

Micro controller based low frequency harmonics elimination using two level cascaded inverter

¹Sundaram A, ²Kibru Mesfin Germamo, ³Bekalu Lakie

Wolkite University, Department of Electrical and Computer Engineering, Wolkite, Ethiopia

Abstract

The low frequency generated in the power system reduces the overall efficiency of the system to a greater extent and also causes various other problems. This project is developed to reduce the harmonics to a greater extent. This involves the implementation of two-level cascaded inverter with the elimination of 3rd and 5th harmonics using micro-controller (P89V51RD2), Multi-level inverters operate with low frequency and highly efficient than PWM inverters because of low switching losses. H-Bridge inverter provides a significant advantage over other multi-level inverter topologies. It consists of less number of components with an optimized circuit layout. The circuit has been simulated in MULTISIM software. MOSFET (IRF630FP) is used as power switching device. Fourier analysis has been made to eliminate the 3rd and 5th harmonics. Opto-coupler (4 pin DIP 817B) provides the necessary gate driving voltage and is used to overcome the common ground problem. The switching sequences are carefully calculated, used effectively. All the MOSFETs are utilized equally and dc sources provide proper input voltage.

Keywords: Cascaded inverter, MOSFET switch, Low frequency harmonics, Fourier analysis

1. Introduction

Any periodic waveform can be shown to be the super position of a fundamental and a set of harmonic components. The magnitudes of these components are obtained by applying Fourier transformation. The frequency of each harmonic component is an integral multiple of its fundamental.

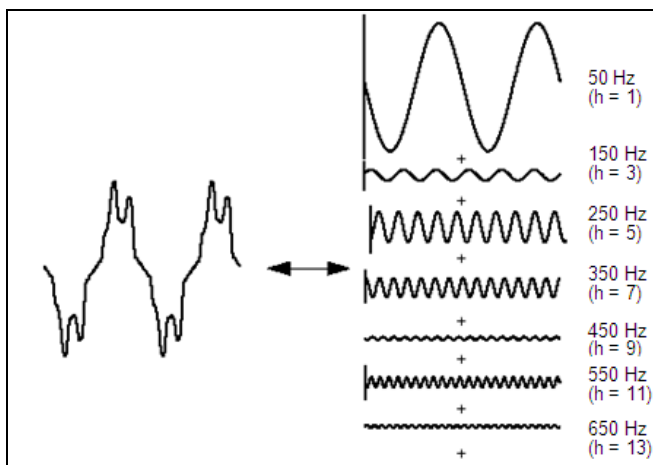


Fig 1: Fourier series representation of a distorted waveform

Filters are used to eliminate harmonics. The size of the filter increases when the order of harmonics decreases. It occupies more space for the increased size of filter, needs cooling system and is cost effective. Hence it is important to eliminate the low frequency harmonics. There are several methods to indicate the quantity of harmonics content. The total harmonic distortion (THD) is a common method to identify the amplitudes of the harmonics (M_h). The function of an inverter is to change a dc input voltage to a symmetric output voltage of desired magnitude and frequency. The output voltage

waveforms of ideal inverters should be sinusoidal. However the waveforms of practical inverters are non-sinusoidal and contain certain harmonics. Generally the inverters can be classified into Voltage source inverters and Current source inverters.

A half-bridge is the simplest topology, which is used to produce a two-level square wave output waveform. A center-tapped voltage source supply is preferred with two-well matched capacitors in series to provide the center tap. The full-bridge topology is used to synthesize a three level square-wave output waveform. The output waveforms of half-bridge and full-bridge of single-phase voltage source inverter are shown in fig 2 and 3 respectively.

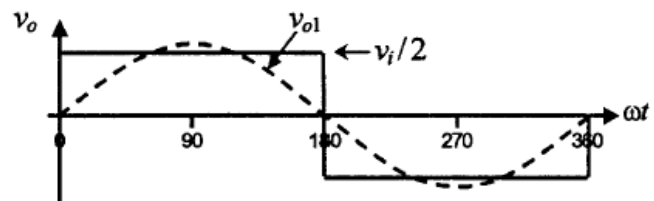


Fig 2: Output waveform of half-bridge configuration

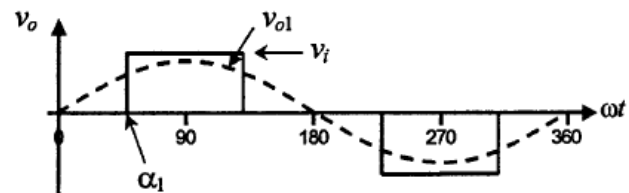


Fig 3: Output waveform of full-bridge configuration

High-switching frequency along with various pulse-width modulation (PWM) strategies is used to obtain a quality output voltage or a current waveform with a minimum

amount of ripple content with limitations in operating under high frequencies mainly due to switching losses and constraints of device ratings.

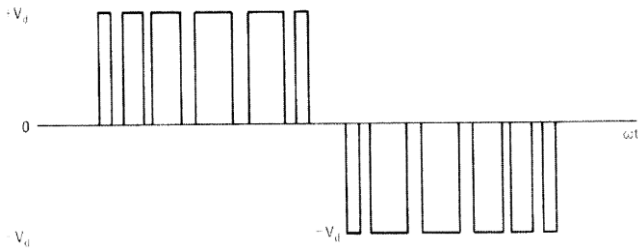


Fig 4: A sinusoidal PWM waveform

2. Cascaded Multi-level inverter

The device is used to develop and to synthesize an approximate sinusoidal waveform from several levels of dc voltages. As the number of voltage levels increase, the synthesized output waveform has more steps, which produces a staircase wave that approaches towards a desired waveform.

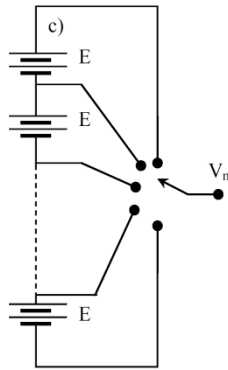


Fig 5: Schematic of multi-level inverter by a switch

The increase in the step of the wave form cause an effect to decrease the harmonic distortion of the output waveform. A series of H-Bridge (single-phase, full-bridge) inverter is used to construct a cascaded multilevel inverter unit. The general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources (SDCSs), which may be obtained from batteries, fuel cells, or solar cells. Fig 6 shows the basic structure of a single-phase cascaded inverter with SDCSs. The ac terminal voltages of different level inverters are connected in series.

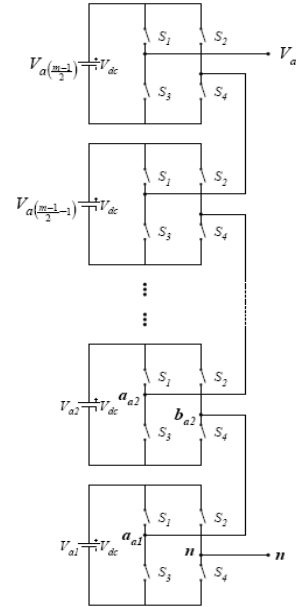


Fig 6: Single-phase multilevel cascaded H-bridge inverter

3. Proposed Inverter

3.1 Circuit Configuration

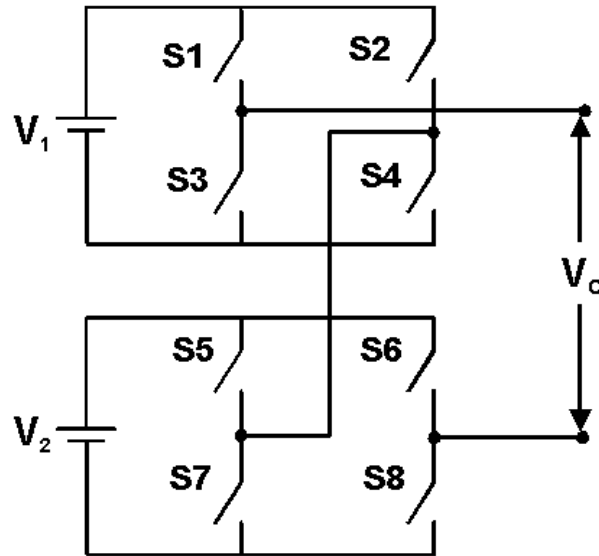


Fig 7: Typical two-level inverter

A typical two-level H-Bridge cascaded inverter with two separate voltage sources V_1 & V_2 and eight power electronic switches is shown in the fig 7. By correctly

switching on and off the appropriate switches at correct instants the desired wave form is obtained as shown in the fig 10.

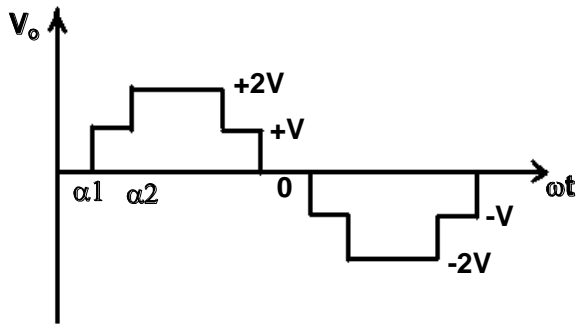


Fig 8: Typical output voltage of a two-level multilevel inverter

The switching sequences must be selected in such a way that both the sources are equally utilized and also all the eight devices are equally used.

Table 1: Switching techniques for various voltage levels

Voltage level	S1	S2	S3	S4	S5	S6	S7	S8
+V (V1)	1	0	0	1	1	1	0	0
	1	0	0	1	0	0	1	1
+V (V2)	1	1	0	0	1	0	0	1
	0	0	1	1	1	0	0	1
+2V	1	0	0	1	1	0	0	1
0V	1	1	0	0	1	1	0	0
	1	1	0	0	0	0	1	1
	0	0	1	1	1	1	0	0
	0	0	1	1	0	0	1	1
-V (V1)	0	1	1	0	1	1	0	0
	0	1	1	0	0	0	1	1
-V (V2)	1	1	0	0	0	1	1	0
	0	0	1	1	0	1	1	0
-2V	0	1	1	0	0	1	1	0

4. Fourier Analysis and Harmonics Elimination

4.1 Fourier Series for Periodic Function

Under steady-state condition, the output voltage of power converters is, generally, a periodic function of time defined by

$$v_o(t) = v_o(t + T) \tag{1}$$

where T is the periodic time. If f is the frequency of the output voltage in hertz, the angular frequency is

$$\omega = 2\pi/T = 2\pi f \tag{2}$$

and Eq.(1) can be rewritten as

$$v_o(\omega t) = v_o(\omega t + 2\pi) \tag{3}$$

The Fourier theorem states that a periodic function $v_o(t)$ can be described by a constant term plus an infinite series of sine and cosine terms of frequency $n\omega$ where n is an integer. Therefore, $v_o(t)$ can be expressed as

$$v_o(t) = a_0/2 + \sum (a_n \cos n\omega t + b_n \sin n\omega t); \tag{4}$$

n varies from 1 to infinity where $a_0/2$ is the average value of the output voltage. The constants a_0 , a_n and b_n can be determined from the following expressions:

$$a_0 = \frac{1}{T} \int_0^T v_o(\omega t) d(\omega t) \tag{5}$$

$$a_n = \frac{1}{\pi} \int_0^{2\pi} v_o(\omega t) \cos n\omega t d(\omega t) \tag{6}$$

$$b_n = \frac{1}{\pi} \int_0^{2\pi} v_o(\omega t) \sin n\omega t d(\omega t) \tag{7}$$

If the output voltage is half-wave symmetry, the number of integrations within the entire period can be reduced significantly. A waveform is half-wave symmetry if the waveform satisfies the following condition:

$$v_o(\omega t) = -v_o(\omega t + \pi) \tag{8}$$

In a waveform with half-wave symmetry. The negative half-wave is a mirror image of the positive half-wave, but phase shifted by T/2 s (or π rad) from the positive half-wave. These do not have even harmonics (i.e., n = 2, 4, 6, ...) and possess only the odd harmonics (i.e., n = 1, 3, 5, ...). Due to the half-wave symmetry, the average value is zero (i.e., $a_0 = 0$). Moreover if the wave is symmetric about y-axis, it contains only cosine terms (i.e., $b_n = 0$) and if the wave is anti-symmetric, it contains only sine terms (i.e., $a_n = 0$).

4.2 Harmonics Elimination

Due to the quarter-wave symmetry along the x-axis, both Fourier coefficients a_0 and a_n are zero. We get b_n as

$$b_n = \frac{4V_{dc}}{\pi} \left[\int_{\alpha_1}^{n/2} \sin n\omega t d(\omega t) + \int_{\alpha_2}^{n/2} \sin n\omega t d(\omega t) \right] \tag{9}$$

$$b_n = \frac{4V_{dc}}{\pi} [\cos n\alpha_1 + \cos n\alpha_2] \tag{10}$$

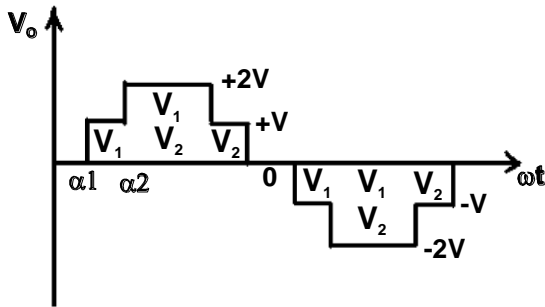
Which gives the instantaneous voltage $v_{on}(\omega t)$ of n^{th} component as

$$v_{on}(\omega t) = \frac{4V_{dc}}{\pi} [\cos n\alpha_1 + \cos n\alpha_2] \sin(n\omega t) \tag{11}$$

The THD of the output voltage is minimized by properly selecting the conducting angles α_1 and α_2 . The conducting angles are selected so as to eliminate the 3rd and 5th harmonics. Initially the simple gauss-siedel iteration method is used to solve the above equations. But iteration starts oscillating between two values. So a slight change is introduced in the normal iteration procedure. A simple C++ program is developed to solve the above equations. The use of micro-controller in this work is to generate accurate on/ off pulses for all the eight MOSFETs. It is very compact, occupies very less space, allows reprogramming of time-delays, and is very reliable. The

P89V51RD2 is an 80C51 microcontroller with 64 kB Flash and 1024 bytes of data RAM.

Switching sequence should be selected so as to equally utilize both the voltage sources and to equally use all the eight MOSFETs. The switching sequence is shown in fig 9. The MOSFETs are equally used, that is, four times per cycle.



MOSFETs switched ON:

- | | |
|--------------------------|--------------------------------|
| 1, 4, 5, 6 - V_1 | 2, 3, 7, 8 - $(-V_1)$ |
| 1, 4, 5, 8 - $V_1 + V_2$ | 2, 3, 6, 7 - $(-V_1) + (-V_2)$ |
| 1, 2, 5, 8 - V_2 | 3, 4, 6, 7 - $(-V_2)$ |
| 1, 2, 5, 6 - $0V$ | 3, 4, 7, 8 - $0V$ |

Fig 9: Switching sequence

Since all the outputs are taken from port 0, it is unable to drive the opto-coupler. To avoid this problem, anode is connected to the source voltage of micro-controller and cathode is connected to the ports. So, to drive an opto-

coupler LED, the port pin should be at 0-level not at 1-level. The port 0 output values are calculated based on the above idea.

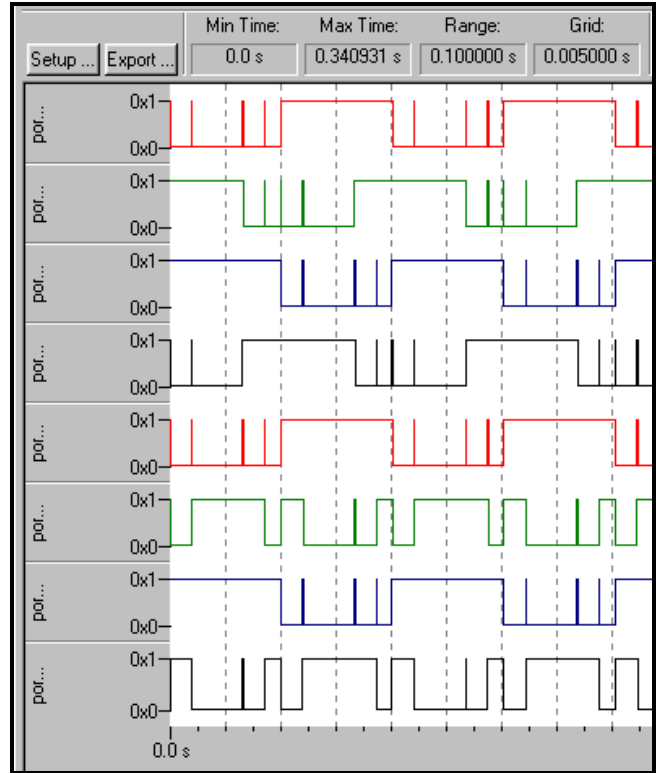


Fig 10: Output waveform of port 0, pins 0-7, from top to down

5. Simulation and hardware implementation

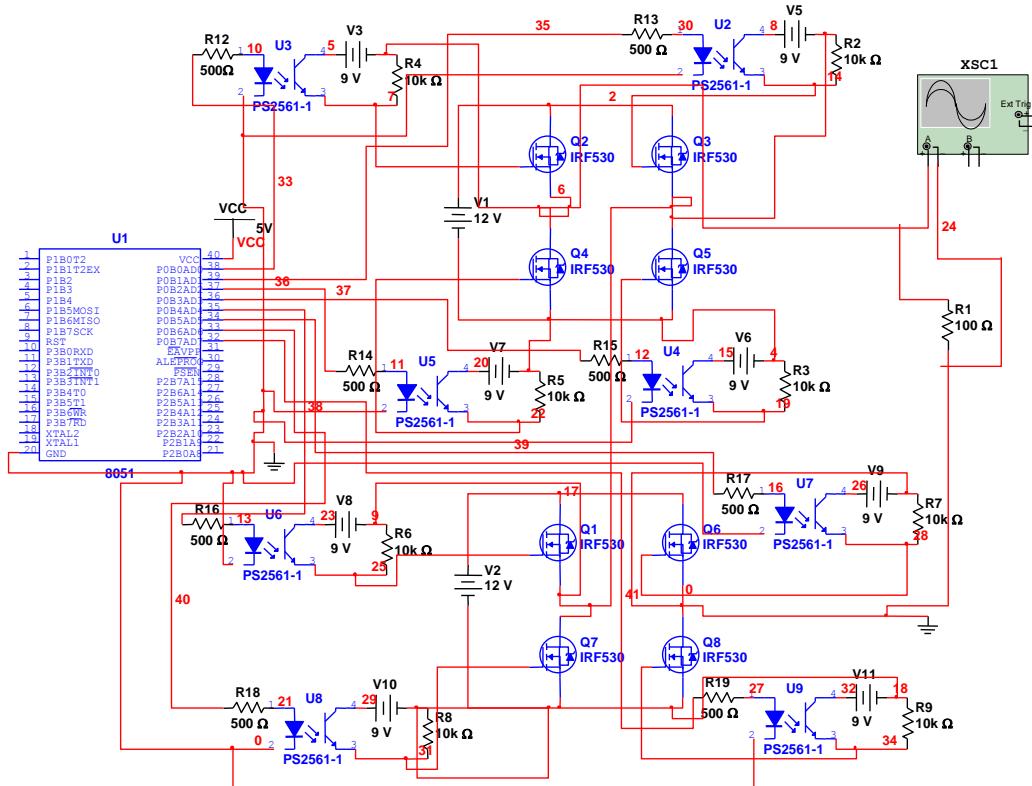


Fig 11: Circuit simulated in MULTISIM

The Fourier analysis has been done in the output (stepped) waveform using MULTISIM software.

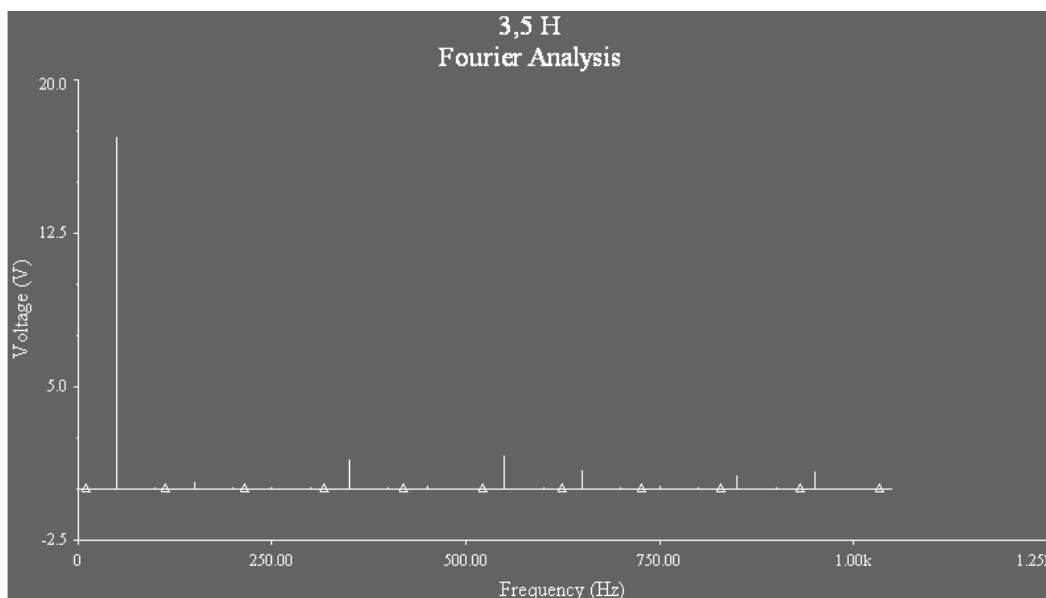


Fig 12: Fourier analysis – Magnitude of each component

Table 2: Magnitude of each harmonic component

Fourier analysis for V(7):					
DC component:	0.00130864				
No. Harmonics:	70				
THD:	16.4158 %				
Gridsize:	2048				
Interpolation Degree:	1				
Harmonic	Frequency	Magnitude	Phase	Norm. Mag	Norm. Phase
1	50	17.1894	0.0192059	1	0
2	100	0.00458722	-142.11	0.000266864	-142.13
3	150	0.304264	-2.2497	0.0177007	-2.2689
4	200	0.00683731	-101.48	0.000397763	-101.5
5	250	0.0987413	-4.3269	0.00574431	-4.3461
6	300	0.000797697	86.1695	4.64063e-005	86.1503
7	350	1.42308	0.441108	0.0827883	0.421902
8	400	0.0061642	125.192	0.000358605	125.173
9	450	0.0424065	173.539	0.00246701	173.52
10	500	0.00456546	-165.06	0.000265598	-165.08
11	550	1.53639	-179.62	0.0893801	-179.64
12	600	0.00213747	-87.623	0.000124348	-87.643
13	650	0.855117	179.943	0.0497467	179.924

14	700	0.00602146	75.4948	0.000350301	75.4756
15	750	0.077446	168.981	0.00450545	168.962
16	800	0.00612191	102.14	0.000356145	102.121
17	850	0.634102	179.887	0.0368891	179.867
18	900	0.00209299	-89.182	0.00012176	-89.201
19	950	0.879304	-179.32	0.0511539	-179.34
20	1000	0.00475357	-19.339	0.000276541	-19.358
21	1050	0.0143393	163.315	0.000834195	163.296
22	1100	0.00595508	52.6391	0.000346439	52.6199
23	1150	0.449732	1.39467	0.0261633	1.37547
24	1200	0.000871074	97.0526	5.06751e-005	97.0334
25	1250	0.0387048	-10.692	0.00225167	-10.711
26	1300	0.00688394	-80.119	0.000400476	-80.138
27	1350	0.0385306	-18.65	0.00224153	-18.669
28	1400	0.00466714	-42.505	0.000271513	-42.525
29	1450	0.588836	0.519977	0.0342558	0.500772
30	1500	0.00261979	93.2234	0.000152408	93.2042
31	1550	0.556692	0.633102	0.0323858	0.613896
32	1600	0.00453712	-147.04	0.000263949	-147.06
33	1650	0.0289536	-23.416	0.00168439	-23.435

From the above table 2 the harmonics dominating are 7, 11, 13, 17, 19, etc.

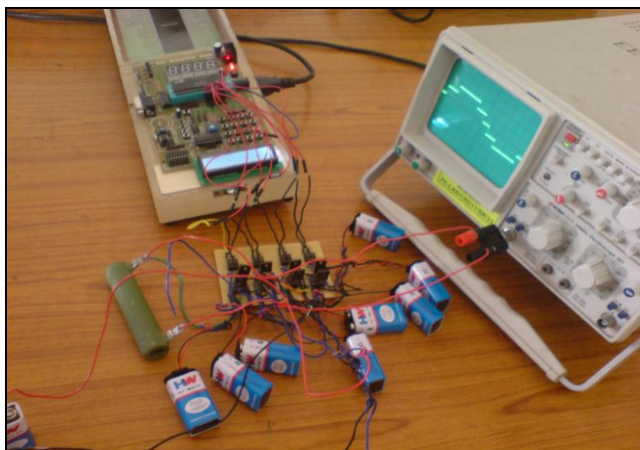


Fig 13: The whole experimental setup

The output of the inverter is connected to a resistive load. The waveform is seen using a CRO.

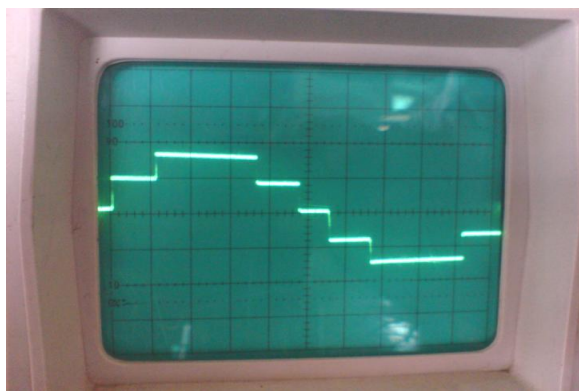


Fig 14: Output waveform

6. Conclusion

The hardware of two-level cascaded inverter was successfully implemented and found that the 3rd and 5th order harmonics are eliminated. It is observed that the required output is achieved. It is found that the system is more suitable for the dc-ac conversion from batteries, fuel cells and solar cells. In this proposal a least number of components are used when compared to the other multilevel inverter topologies. Optimizing the circuit layout and packaging are easily possible because the circuits for all the levels are same. This two-level inverter has only 8 transitions in each cycle, but a PWM inverter of same type needs 10 transitions. Moreover in each transition only half of the voltage is applied across the MOSFET so switching loss is halved. Thus switching loss is substantially reduced when compared to PWM inverters.

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